UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/749,825	12/28/2000	John Alson Hicks III	00216	5201

38516   7590   06/05/2012
AT&T Legal Department - SZ
Attn: Patent Docketing
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EXAMINER
SALTARELLI, DOMINIC D

ART UNIT	PAPER NUMBER
2421	

MAIL DATE	DELIVERY MODE
06/05/2012	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

PTOL-90A (Rev. 04/07)

	Application No.	Applicant(s)
Office Action Summary	09/749,825	HICKS ET AL.
	Examiner	Art Unit	
	DOMINIC D. SALTARELLI	2421	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>25 May 2012</u>.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____ ; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

5)☒ Claim(s) <u>1,5-14,36,39-46 and 52</u> is/are pending in the application.

   5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) <u>1,5-14,36,39-46 and 52</u> is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

   Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

   Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

12)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   a)☐ All b)☐ Some * c)☐ None of:

     1.☐ Certified copies of the priority documents have been received.

     2.☐ Certified copies of the priority documents have been received in Application No. _____ .

     3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

   * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO/SB/08)
   Paper No(s)/Mail Date _____ .

4)☐ Interview Summary (PTO-413)
   Paper No(s)/Mail Date. _____ .

5)☐ Notice of Informal Patent Application

6)☐ Other: _____ .

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1.   A request for continued examination under 37 CFR 1.114, including the fee set

forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this

application is eligible for continued examination under 37 CFR 1.114, and the fee set

forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action

has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on May 25,

2012 has been entered.

Response to Arguments

2.   Applicant's arguments with respect to claims 1, 5-14, 36, 39-46, and 52 have

been considered but are moot because the arguments do not apply to any of the

references being used in the current rejection.

Claim Rejections - 35 USC § 112

3.   The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of
> making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the
> art to which it pertains, or with which it is most nearly connected, to make and use the same and shall
> set forth the best mode contemplated by the inventor of carrying out his invention.

4.   Claims 1, 5-14, 36, 39-46, and 52 are rejected under 35 U.S.C. 112, first

paragraph, as failing to comply with the written description requirement. The claims

contains subject matter which was not described in the specification in such a way as to

reasonably convey to one skilled in the relevant art that the inventors, at the time the

application was filed, had possession of the claimed invention. Each of the independent

claims 1, 36, and 52 has been amended to recite the limitation of dedicating a port on

the data switch to each pair of tuner and demodulators, as supported by the originally

filed specification on page 16, lines 7-11, and using dedicated ports as disclosed

involves using dedicated links (dedicated link 146, shown in fig. 2). This embodiment is

disclosed as an alternate embodiment to using a shared communications link or shared

system bus (145 and 135, respectively, see page 16, lines 11-13). The claims further

recite the tuner/demodulator pairs each output a plurality of signals onto a single media

bus, which has outputs that connect to a video overlay processor which receives the

plurality of signals from this media bus which is claimed to be connected to each of the

tuner/demodulator pairs, which defines the media bus as being a shared bus according

to the second disclosed embodiment on page 16. There is no disclosure in the originally

filed specification which suggests using both dedicated links and a shared bus within a

single embodiment. Claims 5-14 and 39-46 are also rejected for being dependent upon

claims 1 and 36, respectively, for containing the same limitations.

Claim Rejections - 35 USC § 103

5.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set
> forth in section 102 of this title, if the differences between the subject matter sought to be patented and
> the prior art are such that the subject matter as a whole would have been obvious at the time the
> invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

6.   Claims 1, 5-14, 36, 39-46, and 52 are rejected under 35 U.S.C. 103(a) as being

unpatentable over Humpleman (6,005,861, of record) in view of Eames et al.

(6,493,875, listed on the IDS filed 7/30/07) [Eames], Russo (6,732,366, of record),

Inoue et al. (4,890,1680, of record) [Inoue], and Medina et al. (6,967,962) [Medina].

Regarding claims 1, 36, 44, and 52, Humpleman discloses a system for

providing digital entertainment data, the system comprising:

a plurality of buses interconnecting internal components of a gateway

(shown in fig. 1, internal network 34 and fig. 7, where the crossbar is found within

a gateway device, col. 5, lines 20-25), the gateway comprising:

a processor and memory connected to a bus of the plurality of buses (a

"master" set top box containing network interface units, routing received media

through itself to the network, thus the processor and memory of this set top box

are connected to the media bus the content is output to, col. 5, lines 20-25,

further the components of the switched hub that has been integrated into the

master set top box itself includes a microprocessor and memory, see fig. 7 and

col. 10, lines 47-67);

multiple pairs of a tuner and demodulator with each pair of the tuner and

demodulator receiving a plurality of information signals (network interface units

32, col. 9, lines 44-64);

decryption logic having an input connected to the multiple tuner pairs to

received encrypted digital information from the multiple pairs and produce

decrypted digital information (col. 7, lines 55-57);

decoder logic having an input connected to an output of the decryption

logic and receiving the decrypted digital information from the decryption logic, the

decoder logic reformatting the decrypted digital information and producing

reformatted digital information (network interface units also perform any

necessary error correction and formatting into Ethernet packets, col. 9, lines 44-

64);

a data switch connected to the bus, the data switch receiving the

information signals and sending the information signals to a plurality of switch

ports (switch hub 38, shown in fig. 2, which comprises crossbar switch 44 which

provides the switch ports that connect the devices, col. 5, lines 26-44) with a port

for sending high-bandwidth information signals from the data switch (such as for

sending video information to set top equipment, see fig. 2).

Humpleman fails to disclose a digital converter connected to the multiple

pairs to receive analog information from the multiple pairs and to produce digital

information, a system data bus connected to the media bus, a video overlay

processor having three video overlay processor inputs and a video overlay

processor output, a first video overlay processor input connected to a second

media bus output of the media bus, a second video overlay processor input

connected to a third media bus output of the media bus, and a third video overlay

processor input connected to the system data bus, the video overlay processor

output connected to the system data bus, the video overlay processor

superimposing a first audio-visual signal over a second audio-video signal to

produce a superimposed signal and outputting the superimposed signal over the

video overlay processor output to the system data bus, a network bus having a

network bus input connected to the system data bus and receiving the

superimposed signal, a mass storage device connected to the system data bus,

and wherein the data switch has a dedicated port for each of the tuner and

demodulator pairs.

In an analogous art, Eames discloses a system for providing digital

entertainment data (fig. 3), and teaches that it is well known to utilize several

interconnected buses to route information within a gateway (col. 5, lines 26-36).

Designation of the buses within the system is a largely arbitrary practice, since

interconnected buses can be considered a single bus or a collection of buses

equally well. Eames simply names buses according to the type of data which

they transport.

It would have been obvious at the time to a person of ordinary skill in the

art to modify the system disclosed by Humpleman to include plural

interconnected buses as taught by Eames. While Humpleman clearly inherently

includes a bus to transport data from the network interface units to the hub,

Eames is evidence that it is obvious to designate plural interconnected buses for

the transport of data. Whether the buses in question are physically distinct and

indirectly coupled or only separate in the abstract sense cannot be determined,

as the claimed media bus, system data bus, and network bus are disclosed in a

sufficiently vague manner to include both possibilities (see fig. 6 of the originally

filed disclosure). Either case is obvious and well known in view of the prior art,
as the sole purpose of a bus is simply to transport data between circuits.

Humpleman and Eames fail to disclose a digital converter connected to
the multiple pairs to receive analog information from the multiple pairs and to
produce digital information, a video overlay processor having three video overlay
processor inputs and a video overlay processor output, a first video overlay
processor input connected to a second media bus output of the media bus, a
second video overlay processor input connected to a third media bus output of
the media bus, and a third video overlay processor input connected to the system
data bus, the video overlay processor output connected to the system data bus,
the video overlay processor superimposing a first audio-visual signal over a
second audio-video signal to produce a superimposed signal and outputting the
superimposed signal over the video overlay processor output to the system data
bus, a mass storage device connected to the system data bus, and wherein the
data switch has a dedicated port for each of the tuner and demodulator pairs.

In an analogous art, Russo discloses a system for providing digital
entertainment data (fig. 2) including a mass storage device coupled to a system
data bus and storing information signals (fig. 2, storage 110, col. 7, lines 36-50),
providing the benefit of stored programming for later playback (col. 3, lines 9-21).

It would have been obvious at the time to a person of ordinary skill in the
art to modify the system disclosed by Humpleman and Eames to include a mass
storage device coupled to the system data bus and storing the information

signals, as taught by Russo, for the benefit of stored programming for later

playback.

Humpleman, Eames, and Russo fail to disclose a digital converter

connected to the multiple pairs to receive analog information from the multiple

pairs and to produce digital information, a video overlay processor having a first

input connected to the media bus, a second input connected the system data

bus, and an output connected to the system data bus, the video overlay

processor superimposing a first audio-visual signal over a second audio-video

signal to produce a superimposed signal and sending the superimposed signal to

the system data bus, and wherein the data switch has a dedicated port for each

of the tuner and demodulator pairs.

In an analogous art, Inoue discloses a system for providing digital

entertainment data that includes disclose a digital converter receiving analog

information and producing digital information (fig. 2, A/D 37), and an overlay

processor having at least 3 inputs and one output superimposing multiple

information signals onto a first information signal (fig. 2, PIP control 34), providing

the benefit of allowing a user to view several sources of video on a screen

simultaneously (see figs. 5a and 5b).

It would have been obvious at the time to a person of ordinary skill in the

art to modify the system disclosed by Humpleman, Eames, and Russo to include

a digital converter receiving analog information and producing digital information,

and an overlay processor having at least 3 inputs and one output superimposing

multiple information signals onto a first information signal, as taught by Inoue, providing the benefit of allowing a user to view several sources of video on a screen simultaneously.

Humplema, Eames, Russo, and Inoue fail to disclose wherein the data switch has a dedicated port for each of the tuner and demodulator pairs.

In an analogous art, Medina discloses it was well known at the time to persons of ordinary skill in the art to dedicate ports of a switch to respective input devices (col. 3, lines 40-57). When implementing a switch in a packet switched system only two options are available, using dedicated ports or dynamic port assignment, thus it would have been obvious at the time to a person of ordinary skill in the art to utilize a switch having dedicated ports given the finite number of solutions available.

Regarding claims 5, 6, 39-41, 43, and 46, Humpleman, Eames, Russo, Inoue, and Medina disclose the system of claims 1 and 36, wherein a mass storage device stores an item identifier corresponding to each stored content item, the item identifier having a value that indicates the content item has been played (for pay-per-play usage, Russo, col. 5, lines 12-21), another value indicated the content items has been purchased (for open ended usage, Russo, col. 5, lines 45-58), a third value indicating the content item has been licensed (available for viewing, Russo, col. 5 line 59 - col. 6 line 9), a cost of playback for each content item (to debit the account for pay-per-play usage, Russo, col. 10,

lines 33-34) and a second cost of purchase for each content item (to debit the

account for open ended usage, Russo, col. 10, lines 33-34), and further disclose

storing in memory a browser based graphical user interface, which upon

instruction from the client device, a processor sends the graphical user interface

to the client device with the graphical user interface describing the content items

stored in the memory, the processor receiving a command from the client device

issued by a remote control, and the processor retrieving another instruction from

the memory that is associated with the command issued by the remote control

(Russo discloses the system provides a browser based user interface which

provides information regarding program usage indicators and other descriptive

data, granting access to stored and otherwise available programming, col. 5 line

59 - col. 6 line 9 and col. 10 line 59 - col. 11 line 15). The examiner recognizes

that the pay-per-play and open ended, or 'rental' paradigm, uses are disclosed as

alternative embodiments in Russo, however, they are not mutually exclusive and

therefore both included when Humpleman and Eames are modified in view of

Russo's disclosure to include the mass storage device.

Regarding claims 7, 8, and 42, Humpleman, Eames, Russo, Inoue, and

Medina disclose the system of claims 1 and 36, but fail to disclose a card reader

having a card reader input and a card reader output, the card reader input

connected to an output of the decryption logic, the card reader providing

authorization for the decryption logic to decrypt the plurality of information signals

to produce decrypted digital information.

Examiner takes official notice that the use of so called "smart cards" to

authorized access to encrypted television programming is notoriously well known

in the art (such as found in U.S. Patent No. 5,635,989 to Rothmuller, col. 3, lines

41-46), said cards having preprogramming access control information (such as

decryption keys) that are inserted into a set top device to enable said device to

decrypt particular transmissions using the information on the card. Said cards

are used to ensure that only the bearer of the card is able to access encrypted

content, which is more secure than sending decryption information over the

network where it could be intercepted by an unauthorized user.

It would have been obvious at the time to a person of ordinary skill in the

art to modify the system of Humpleman, Eames, Russo, Inoue, and Medina to

include a card reader having a card reader input and a card reader output, the

card reader input connected to an output of the decryption logic, the card reader

providing authorization for the decryption logic to decrypt the plurality of

information signals to produce decrypted digital information.

Regarding claim 9, Humpleman, Eames, Russo, Inoue, and Medina

disclose the system of claim 8, further comprising decoder logic connected to the

media bus (Humpleman teaches the network interface units that are located at

the gateway device perform all necessary decoding functions [decryption, access

control, demultiplexing, etc...] prior to transmission over the bus to the switch,
col. 7, lines 55-65).

Regarding claims 10-14, Humpleman, Eames, Russo, Inoue, and Medina
disclose the system of claim 9, wherein the plurality of transmission signals
include a plurality of television program signals (digital or mixed analog/digital
broadcast signals), an audio signal (compressed audio), a data signal (Internet
data), are received from a cable headend or direct broadcast satellite (cable
provider or digital satellite service), and are frequency divided multplex
transmission signals (as is conventional for cable and satellite television
broadcast services, Humpleman, col. 3, lines 21-35).

Regarding claim 45, Humpleman, Eames, Russo, Inoue, and Medina
disclose the method of claim 36, wherein the data switch is a router
(Humpleman, col. 5, lines 50-59).

Conclusion

Any inquiry concerning this communication or earlier communications from the
examiner should be directed to DOMINIC D. SALTARELLI whose telephone number is
(571)272-7302. The examiner can normally be reached on Monday - Friday 9:00am -
6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kristine Kincaid can be reached on (571) 272-4063. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Dominic D Saltarelli/
Primary Examiner, Art Unit 2421